Single-chip Type with built-in FET Switching Regulator Series

Flexible Step-down Switching Regulators with Built-in Power MOSFET

BD9778F, BD9778HFP, BD9001F, BD9781HFP   No.10027EBT41

● Overview

The flexible step-down switching regulator controller is a switching regulator controller designed with a high-withstand-voltage built-in POWER MOS FET, providing a free setting function of operating frequency with external resistor. This switching regulator controller features a wide input voltage range (7 V to 35 V or 7 V to 48 V) and operating temperature range (-40˚C to +125˚C or -40˚C to +95˚C). Furthermore, an external synchronization input pin (BD9781HFP) enables synchronous operation with external clock.

● Features

1) Minimal external components
2) Wide input voltage range: 7 V to 35 V (BD9778F/HFP and BD9781HFP), 7 V to 48 V (BD9001F)
3) Built-in P-ch POWER MOS FET
4) Output voltage setting enabled with external resistor: 1 to V_{IN}
5) Reference voltage accuracy: ±2%
6) Wide operating temperature range: -40˚C to +125˚C (BD9778F/HFP and BD9781HFP),
                                                                    -40˚C to +95˚C (BD9001F)
8) Low dropout: 100% ON Duty cycle
9) Standby mode supply current: 0 µA (Typ.) (BD9778F/HFP and BD9781HFP), 4 µA (Typ.) (BD9001F)
10) Oscillation frequency variable with external resistor: 50 to 300 kHz (BD9001F),
       50 to 500 kHz (BD9778F/HFP and BD9781HFP)
11) External synchronization enabled (only on the BD9781HFP)
12) Soft start function : soft start time fixed to 5 ms (Typ.))
13) Built-in overcurrent protection circuit
14) Built-in thermal shutdown protection circuit
15) High power HRP7 package mounted (BD9778HFP and BD9781HFP)
      Compact SOP8 package mounted (BD9778F and BD9001F)

● Applications

All fields of industrial equipment, such as Flat TV , printer, DVD, car audio, car navigation, and communication such as ETC, AV, and OA.

● Product lineup

Item	BD9778F/HFP	BD9001F	BD9781HFP
Output current	2A	2A	4A
Input range	7V ~ 35V	7V ~ 48V	7V ~ 35V
Oscillation frequency range	50 ~ 500kHz	50 ~ 300kHz	50 ~ 500kHz
External synchronization	Not provided	Not provided	Provided
Standby function	Provided	Provided	Provided
Operating temperature	−40˚C ~ +125˚C	−40˚C ~ +95˚C	−40˚C ~ +125˚C
Package	SOP8 / HRP7	SOP8	HRP7

● Absolute Maximum Ratings(Ta = 25°C)

Parameter		Symbol	Limits		Unit
Power supply voltage	BD9778F/HFP,BD9781HFP	V_{IN}	36		V
	BD9001F		50		
Output switch pin voltage		V_{SW}	V_{IN}		V
Output switch current	BD9778F/HFP, BD9001F	I_{SW}	2	*1	A
	BD9781HFP		4	*1	
EN/SYNC, EN pin voltage		$V_{EN/SYNC}, V_{EN}$	V_{IN}		V
RT, FB, INV pin voltage		V_{RT}, V_{FB}, V_{INV}	7		
Power dissipation	HRP7	P_d	5.5	*2	W
	SOP8		0.69	*3	
Operating temperature range	BD9778F/HFP,BD9781HFP	T_{opr}	−40 ~ +125		°C
	BD9001F		−40 ~ +95		
Storage temperature range		T_{stg}	−55 ~ +150		°C
Maximum junction temperature		T_{jmax}	150		°C

*1 Should not exceed Pd-value.
*2 Reduce by 44mW/°C over 25°C, when mounted on 2-layer PCB of 70 X 70 X 1.6 mm3.
(PCB incorporates thermal via. Copper foil area on the front side of PCB: 10.5 X 10.5 mm2. Copper foil area on the reverse side of PCB: 70 X 70 mm2)
*3 Reduce by 5.52 mW/°C over 25°C, when mounted on 2-layer PCB of 70 X 70 X 1.6 mm3.

● Recommended operating range

Parameter	BD9778F/HFP	BD9001F	BD9781HFP	Unit
Operating power supply voltage	7 ~ 35	7 ~ 48	7 ~ 35	V
Output switch current	~ 2	~ 2	~ 4	A
Output voltage (ON Duty)	6 ~ 100	6 ~ 100	6 ~ 100	%
Oscillation frequency	50 ~ 500	50 ~ 300	50 ~ 500	kHz
Oscillation frequency set resistance	40 ~ 800	100 ~ 800	39 ~ 800	kΩ

● Possible operating range

Parameter	BD9778F/HFP	BD9001F	BD9781HFP	Unit
Operating power supply voltage	5 ~ 35	7 ~ 48	5 ~ 35	V

● Electrical characteristics
◎BD9778F/HFP (Unless otherwise specified, Ta = -40°C to +125°C, V_{IN} =13.2 V, V_{EN} = 5 V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Standby circuit current	I_{STB}	–	0	10	μA	V_{EN}=0V,Ta=25°C
Circuit current	I_Q	–	3	4.2	mA	I_O=0A
[SW block]						
POWER MOS FET ON resistance	R_{ON}	–	0.53	0.9	Ω	I_{SW}=50mA
Operating output current of overcurrent protection	I_{OLIMIT}	2	4	–	A	* Design assurance
Output leak current	I_{OLEAK}	–	0	30	μA	V_{IN}=35V,V_{EN}=0V
[Error Amp block]						
Reference voltage 1	V_{REF1}	0.98	1.00	1.02	V	V_{FB}=V_{INV},Ta=25°C
Reference voltage 2	V_{REF2}	0.96	1.00	1.04	V	V_{FB}=V_{INV}
Reference voltage input regulation	ΔV_{REF}	–	0.5	–	%	V_{IN}=5 ~ 35V
Input bias current	I_B	−1	–	–	μA	V_{INV}=1.1V
Maximum FB voltage	V_{FBH}	2.4	2.5	–	V	V_{INV}=0.5V
Minimum FB voltage	V_{FBL}	–	0.05	0.10	V	V_{INV}=1.5V
FB sink current	I_{FBSINK}	−5.0	−3.0	−0.5	mA	V_{FB}=1.5V,V_{INV}=1.5V
FB source current	$I_{FBSOURCE}$	70	120	170	μA	V_{FB}=1.5V,V_{INV}=0.5V
Soft start time	T_{SS}	–	5	–	mS	* Design assurance
[Oscillator block]						
Oscillation frequency	F_{OSC}	82	102	122	kHz	R_T=390kΩ
Frequency input regulation	ΔF_{OSC}	–	1	–	%	V_{IN}=5 ~ 35V
[Enable block]						
Threshold voltage	V_{EN}	0.8	1.7	2.6	V	
Sink current	I_{EN}	–	13	50	μA	V_{EN}=5V

* Not designed to be radiation-resistant.

◎BD9001F (Unless otherwise specified, Ta=−40˚C ~ +95˚C, V_{IN}=13.2V, V_{EN}=5V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Standby circuit current	I_{STB}	–	4	10	µA	V_{EN}=0V,Ta=25˚C
Circuit current	I_Q	–	3	4.2	mA	I_O=0A
[SW block]						
POWER MOS FET ON resistance	R_{ON}	–	0.6	1.2	Ω	I_{SW}=50mA
Operating output current of overcurrent protection	I_{OLIMIT}	2.5	4	–	A	* Design assurance
[Error Amp block]						
Reference voltage 1	V_{REF1}	0.98	1.00	1.02	V	V_{FB}=V_{INV},Ta=25˚C
Reference voltage 2	V_{REF2}	0.96	1.00	1.04	V	V_{FB}=V_{INV}
Reference voltage input regulation	ΔV_{REF}	–	0.5	–	%	V_{IN}=7 ~ 48V
Input bias current	I_B	−1	–	–	µA	V_{INV}=1.1V
Maximum FB voltage	V_{FBH}	2.4	2.5	–	V	V_{INV}=0.5V
Minimum FB voltage	V_{FBL}	–	0.05	0.10	V	V_{INV}=1.5V
FB sink current	I_{FBSINK}	−5.0	−3.0	−0.5	mA	V_{FB}=1.5V,V_{INV}=1.5V
FB source current	$I_{FBSOURCE}$	70	120	170	µA	V_{FB}=1.5V,V_{INV}=0.5V
Soft start time	T_{SS}	–	5	–	ms	* Design assurance
[Oscillator block]						
Oscillation frequency	F_{OSC}	82	102	122	kHz	R_T=390kΩ
Frequency input regulation	ΔF_{OSC}	–	2	–	%	V_{IN}=7 ~ 48V
[Enable block]						
Threshold voltage	V_{EN}	0.8	1.7	2.6	V	
Sink current	I_{EN}	–	13	50	µA	V_{EN}=5V

* Not designed to be radiation-resistant.

◎BD9781HFP (Unless otherwise specified, Ta=−40˚C ~ +125˚C, V_{IN}=13.2V, $V_{EN/SYNC}$=5V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Standby circuit current	I_{STB}	–	0	10	µA	$V_{EN/SYNC}$=0V,Ta=25ºC
Circuit current	I_Q	–	3	8	mA	I_O=0A
[SW block]						
POWER MOS FET ON resistance	R_{ON}	–	0.5	0.9	Ω	I_{SW}=50mA
Operating output current of overcurrent protection	I_{OLIMIT}	4	8	–	A	* Design assurance
Output leak current	I_{OLEAK}	–	0	30	µA	V_{IN}=35V,$V_{EN/SYNC}$=0V
[Error Amp block]						
Reference voltage1	V_{REF1}	0.98	1.00	1.02	V	V_{FB}=V_{INV},Ta=25ºC
Reference voltage2	V_{REF2}	0.97	1.00	1.03	V	V_{FB}=V_{INV}
Reference voltage input regulation	ΔV_{REF}	–	0.5	–	%	V_{IN}=5 ~ 35V
Input bias current	I_B	−1	–	–	µA	V_{INV}=1.1V
Maximum FB voltage	V_{FBH}	2.4	2.5	–	V	V_{INV}=0.5V
Minimum FB voltage	V_{FBL}	–	0.05	0.10	V	V_{INV}=1.5V
FB sink current	I_{FBSINK}	−5.0	−3.0	−0.5	mA	V_{FB}=1.5V,V_{INV}=1.5V
FB source current	$I_{FBSOURCE}$	70	120	170	µA	V_{FB}=1.5V,V_{INV}=0.5V
Soft start time	T_{SS}	–	5	–	mS	* Design assurance
[Oscillator block]						
Oscillation frequency	F_{OSC}	82	102	122	kHz	R_T=390kΩ
Frequency input regulation	ΔF_{OSC}	–	1	–	%	V_{IN}=5 ~ 35V
[Enable/Synchronizing input block]						
Threshold voltage	$V_{EN/SYNC}$	0.8	1.7	2.6	V	
Sink current	$I_{EN/SYNC}$	–	35	90	µA	$V_{EN/SYNC}$=5V
External synchronizing frequency	F_{SYNC}	–	150	–	kHz	$F_{EN/SYNC}$=150kHz

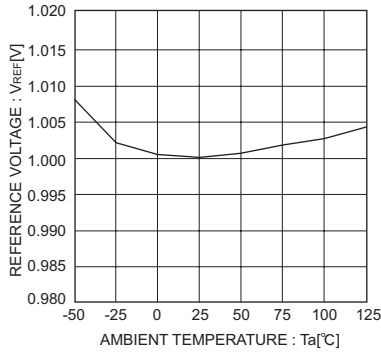* Not designed to be radiation-resistant.

● Reference data

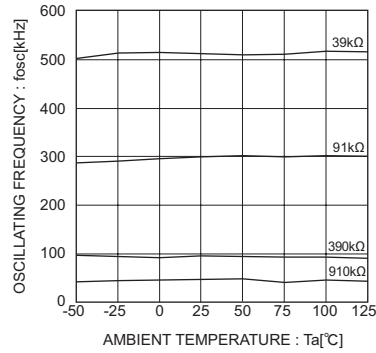Fig.1 Output reference voltage vs. Ambient temprature(All series)

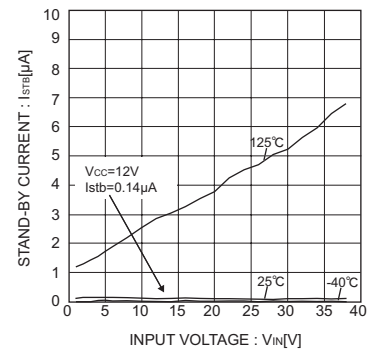Fig.2 Frequency vs. Ambient temperature(All series)

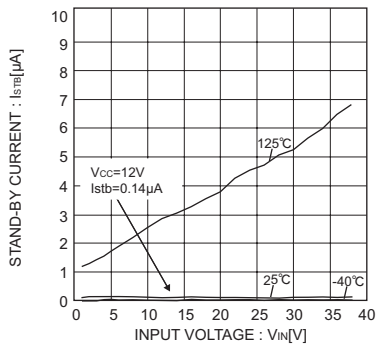Fig.3 Standby current(BD9781HFP)

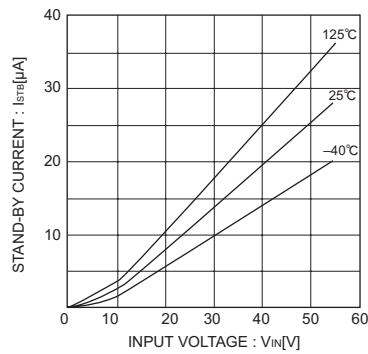Fig.4 Standby current(BD9778F/HFP)

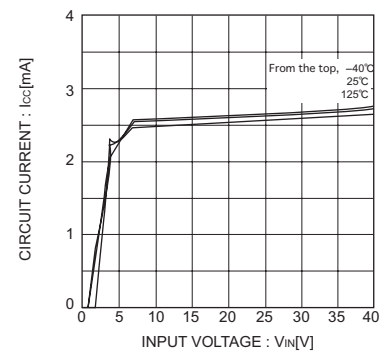

Fig.5 Standby current(BD9001F)
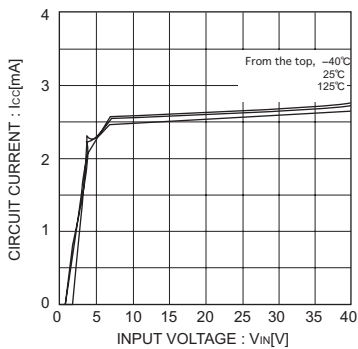

Fig.6 Circuit current(BD9781HFP)
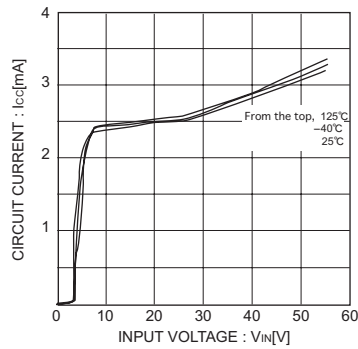

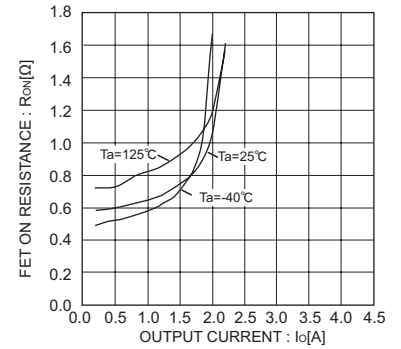Fig.7 Circuit current(BD9778F/HFP)

Fig.8 Circuit current(BD9001F)

Fig.9 ON resistance V_{IN}=5V(BD9781HFP)
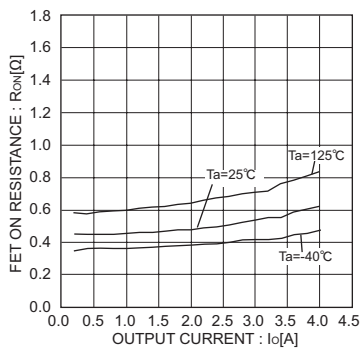
Fig.10 ON resistance V_{IN}=7V (BD9781HFP)
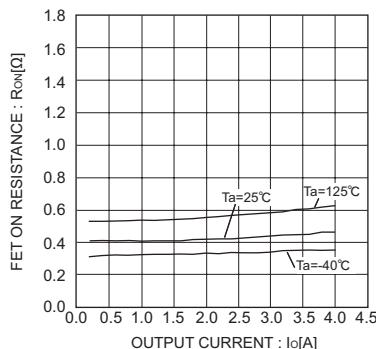
Fig.11 ON resistanceV_{IN}=13.2V (BD9781HFP)
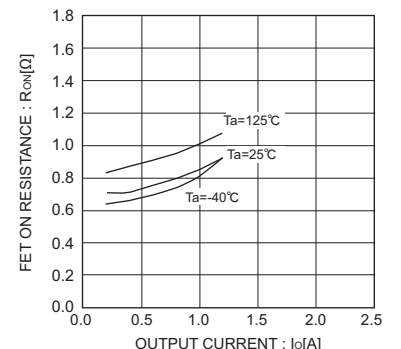
Fig.12 ON resistance V_{IN}=5V (BD9778F/HFP)
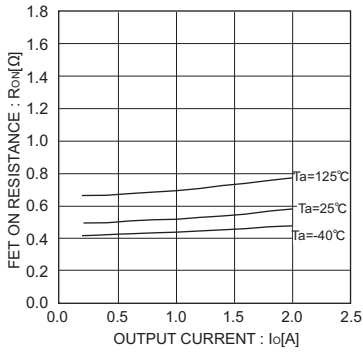
Fig.13 ON resistance V$_{IN}$=7V (BD9778F/HFP)
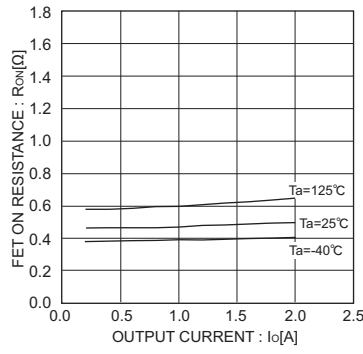
Fig.14 ON resistance V$_{IN}$=13.2V (BD9778F/HFP)
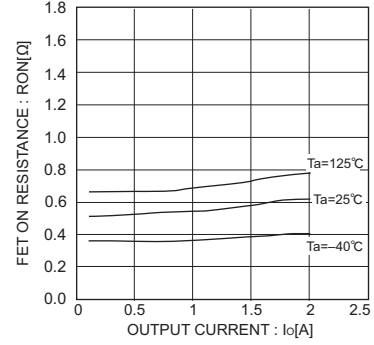
Fig.15 ON resistance V$_{IN}$=7V (BD9001F)
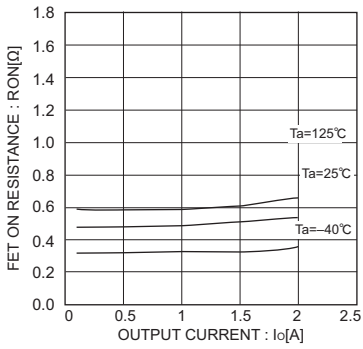
Fig.16 ON resistance V$_{IN}$=13.2V (BD9001F)
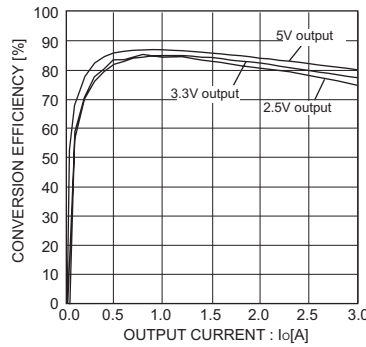
Fig.17 I$_O$ vs Efficiency(V$_{IN}$=12V,f=200kHz) (BD9781HFP)
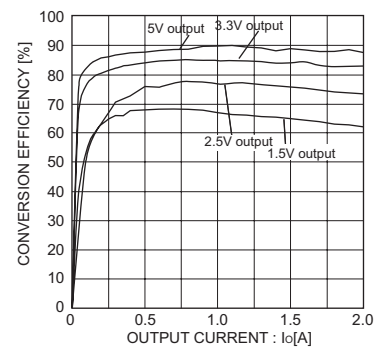
Fig.18 I$_O$ vs Efficiency(V$_{IN}$=12V,f=100kHz) (BD9778F/HFP)
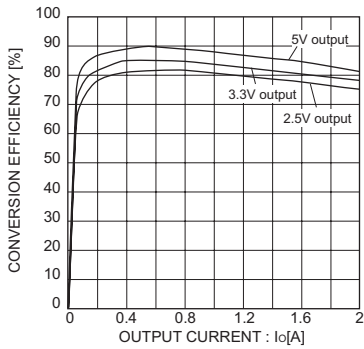
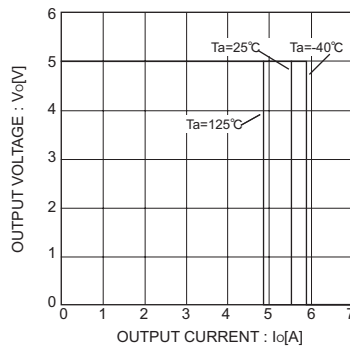Fig.19 I$_O$ vs Efficiency(V$_{IN}$=12V,f=100kHz) (BD9001F)

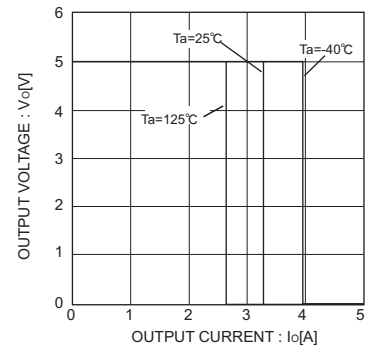Fig.20 Current capacitance(V$_{IN}$=12V,Vo=5V,f=100kHz) (BD9781HFP)

Fig.21 Current capacitance(V$_{IN}$=12V,Vo=5V,f=100kHz) (BD9778F/HFP)
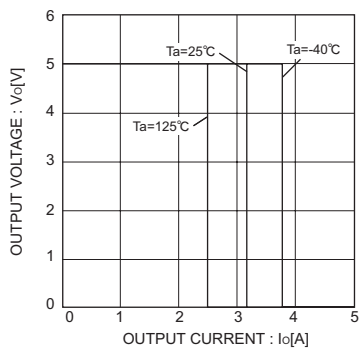
Fig.22 Current capacitance(V$_{IN}$=12V,Vo=5V,f=100kHz) (BD9001F)

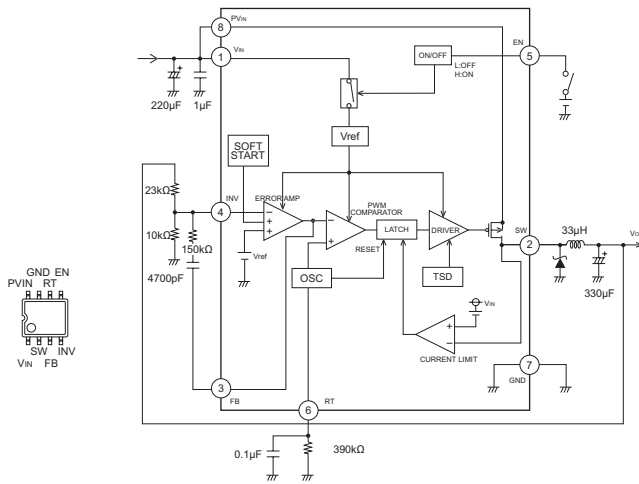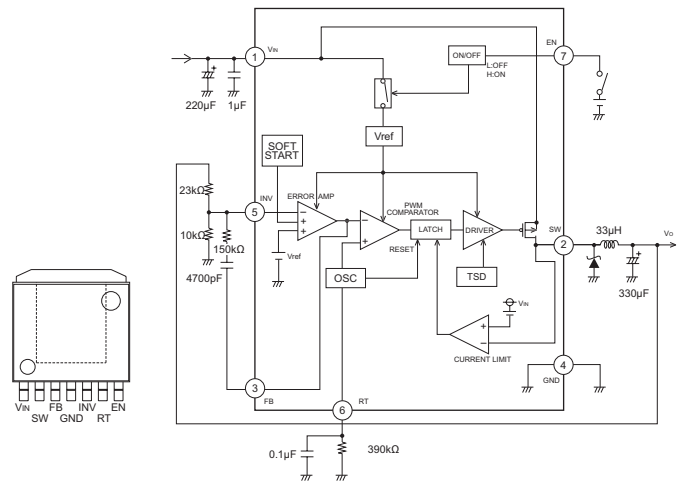● Block diagram / Application circuit / Pin assignment

(BD9778F)

Fig.23

No.	Pin name	Function
1	VIN	Power supply input
2	SW	Output
3	FB	Error Amp output
4	INV	Output voltage feedback
5	EN	Enable
6	RT	Frequency setting resistor connection
7	GND	Ground
8	PVIN	Power system power supply input

(BD9778HFP)

Fig.24

No.	Pin name	Function
1	VIN	Power supply input
2	SW	Output
3	FB	Error Amp output
4	GND	Ground
5	INV	Output voltage feedback
6	RT	Frequency setting resistor connection
7	EN	Enable
FIN	–	Ground

(BD9001F)

Fig.25
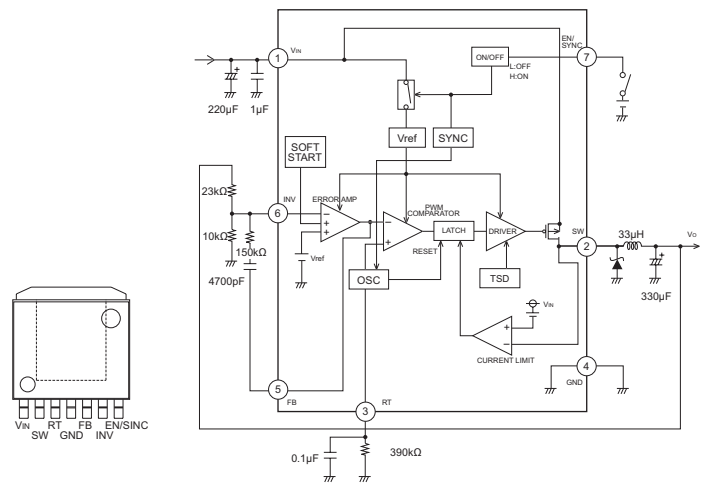
No.	Pin name	Function
1	SW	Output
2	N.C.	Non Connection
3	FB	Error Amp Output
4	INV	Output voltage feedback
5	EN	Enable
6	RT	Frequency setting resistor connection
7	GND	Ground
8	VIN	Power supply input

(BD9781HFP)

Fig.26

No.	Pin name	Function
1	VIN	Power supply input
2	SW	Output
3	RT	Frequency setting resistor connection
4	GND	Ground
5	FB	Error Amp output
6	INV	Output voltage feedback
7	EN/SYNC	Enable/Synchronizing pulse input
FIN	–	Ground

● Description of operations

・ERROR AMP
    The ERROR AMP block is an error amplifier used to input the reference voltage (1 V typ.) and the INV pin voltage. The output FB pin controls the switching duty and output voltage Vo. These INV and FB pins are externally mounted to facilitate phase compensation. Inserting a capacitor and resistor between these pins enables adjustment of phase margin. (Refer to recommended examples on page 11.)

・SOF T START
    The SOFT START block provides a function to prevent the overshoot of the output voltage Vo through gradually increasing the normal rotation input of the error amplifier when power supply turns ON to gradually increase the switching Duty. The soft start time is set to 5 msec (Typ.).

・ON/OFF(BD9778F/HF P,BD9781HFP)
    Setting the EN pin to 0.8 V or less makes it possible to shut down the circuit. Standby current is set to 0 μA (Typ.). Furthermore, on the BD9781HFP, applying a pulse having a frequency higher than set oscillation frequency to the EN/SYNC pin allows for external synchronization (up to +50% of the set frequency).

・PWM COM PARATOR
    The PWM COMPARATOR block is a comparator to make comparison between the FB pin and internal triangular wave and output a switching pulse.
    The switching pulse duty varies with the FB value and can be set in the range of 0 to 100%.

・OSC(Oscillator)
    The OSC block is a circuit to generate a triangular wave that is to be input in the PWM comparator. Connecting a resistor to the RT pin enables setting of oscillation frequency.

・TSD(Thermal Shut Down)
    In order to prevent thermal destruction/thermal runaway of this IC, the TSD block will turn OFF the output when the chip temperature reaches approximately 150˚C or more. When the chip temperature falls to a specified level, the output will be reset. However, since the TSD is designed to protect the IC, the chip junction temperature should be provided with the thermal shutdown detection temperature of less than approximately 150˚C.

・CURREN T LIMIT
    While the output POWER P-ch MOS FET is ON, if the voltage between drain and source (ON resistance ¥ load current) exceeds the reference voltage internally set with the IC, this block will turn OFF the output to latch. The overcurrent protection detection values have been set as shown below:
        BD9781HFP . . . 8A(Typ.)
        BD9001F,BD9778F/HFP . . . 4A(Typ.)

    Furthermore, since this overcurrent protection is an automatically reset, after the output is turned OFF and latched, the latch will be reset with the RESET signal output by each oscillation frequency.

    However, this protection circuit is only effective in preventing destruction from sudden accident. It does not support for the continuous operation of the protection circuit (e.g. if a load, which significantly exceeds the output current capacitance, is normally connected). Furthermore, since the overcurrent protection detection value has negative temperature characteristics, consider thermal design.

● Timing chart
  (BD9781HFP)
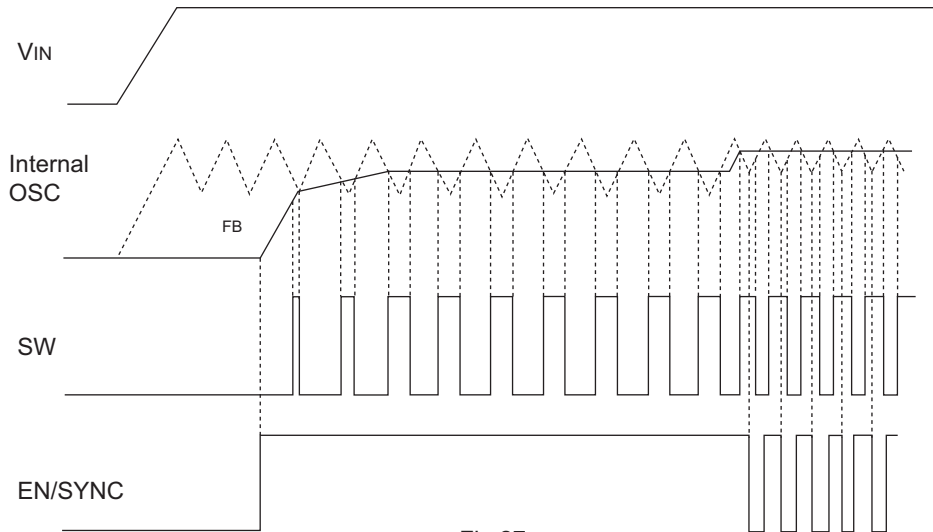 - While in basic operation mode
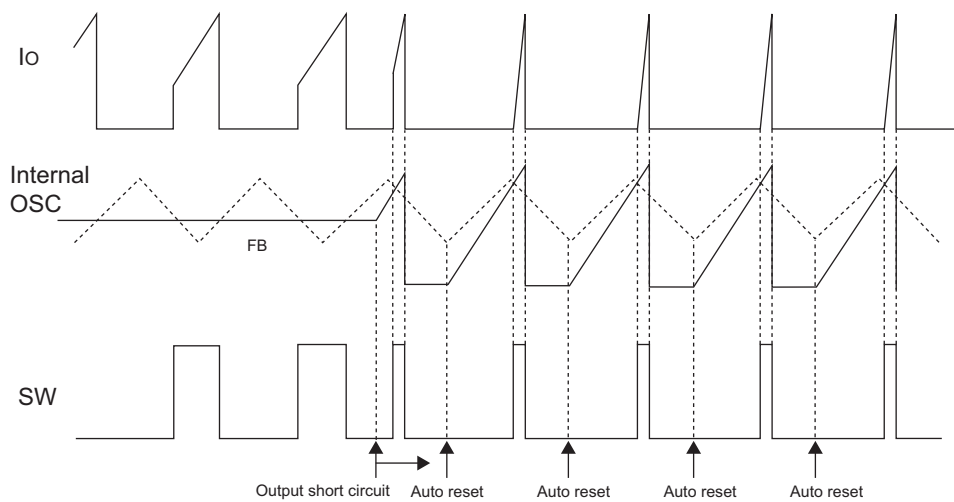

Fig.27

  - While in overcurrent protection mode

Fig.28

● External synchronizing function (BD9781HFP)
  In order to activate the external synchronizing function, connect the frequency setting resistor to the RT pin and then input
  a synchronizing signal to the EN/SYNC pin. As the synchronizing signal, input a pulse wave higher than a frequency determined
  with the setting resistor (RT). On the BD9781HFP, design the frequency difference to be within 50%. Furthermore,
  set the pulse wave duty between 10% and 90%.
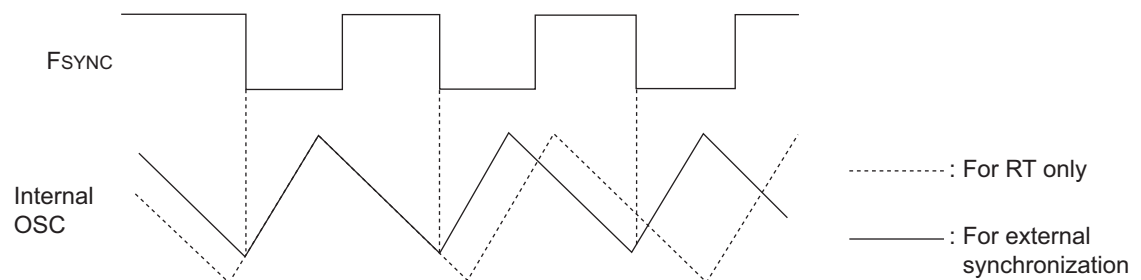
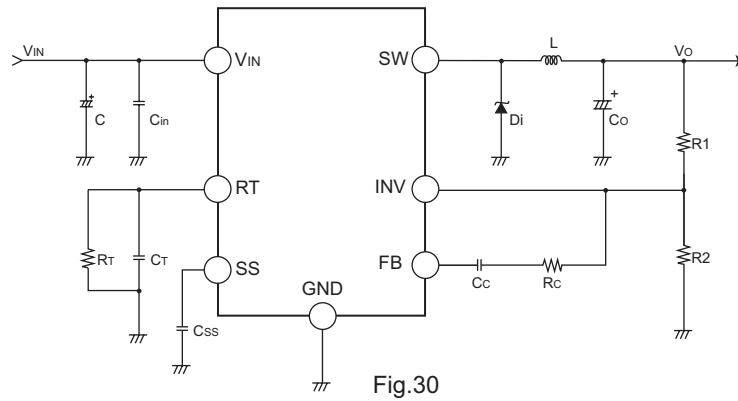

Fig.29

● Description of external components

Fig.30

Design procedure	Calculation example
Vo = Output voltage, Vin (Max.) = Maximum input voltage Io (Max.) = Maximum load current, f = Oscillation frequency	

1. Setting or output voltage
  Output voltage can be obtained by the formula shown below.
 	
    $V_O = 1 \times (1 + R1/R2)$
 	
  Use the formula to select the R1 and R2.
  Furthermore, set the R2 to 30 kΩ or less.
  Select the current passing through the R1 and R2 to be small
  enough for the output current.
	When Vo = 5 V and R2 = 10 kΩ,
	
	    $5 = 1 \times (1 + R1/10k\Omega)$
	
	                                                  R1=40kΩ

2. Selection of coil (L)
  The value of the coil can be obtained by the formula shown
  below:
 	
    $L = (V_{IN} - V_O) \times V_O / (V_{IN} \times f \times \Delta I_O)$
    ΔI_O: Output ripple current
    f = Operating frequency
    ΔI_O should typically be approximately 20 to 30% of Io.
 	
If this coil is not set to the optimum value, normal (continuous)
oscillation may not be achieved. Furthermore, set the value of
the coil with an adequate margin so that the peak current passing
through the coil will not exceed the rated current of the coil.
	When V_{IN} = 13.2 V, Vo = 5 V, Io = 2 A, and f = 100 kHz,
	$L = (13.2-5) \times 5/13.2 \times 1/100k \times 1/(2 \times 0.3)$
	$= 51.8\mu H \fallingdotseq 47\mu$
	
	                                                  L=47μH

3. Selection of output capacitor (Co)
  The output capacitor can be determined according to the
  output ripple voltage ΔVo (p-p) required.
  Obtain the required ESR value by the formula shown below
  and then select the capacitance.
 	
    $\Delta IL = (V_{IN} - V_O) \times V_O/(L \times f \times V_{IN})$
    $\Delta Vpp = \Delta IL \times ESR + (\Delta IL \times Vo)/(2 \times Co \times f \times V_{IN})$
 	
Set the rating of the capacitor with an adequate margin to the
output voltage. Also, set the maximum allowable ripple current
with an adequate margin to ΔIL. Furthermore, the output rise
time should be shorter than the soft start time. Select the output
capacitor having a value smaller than that obtained by the
formula shown below.
 	
    $C_{Max} = \dfrac{3.5m \times (I_{Limit} - Io(Max))}{Vo}$
 	
I_{Limit}:2A(BD9778F/HFP,BD9001F), 4A(BD9781HFP)
If this capacitance is not optimum, faulty startup may result.
 	
(※3.5m is soft start time(min.))
	V_{IN}=13.2V, Vo=5V, L=100μH, f=100kHz
	$\Delta IL = (13.2-5) \times 5/(100 \times 10_{-6} \times 100 \times 10_3 \times 13.2)$
	  $\fallingdotseq 0.31$ ΔIL=0.31A
	
	When I_{Limit}: 2 A, Io (Max) = 1 A, and Vo = 5V,
	
	$C_{Max} = 3.5m \times (2-1)/5$
	    $= 700\mu$
	
	                                                  CMax=700μF

Design procedure	Calculation example

4. Selection of diode
   Set diode rating with an adequate margin to the maximum load
   current. Also, make setting of the rated inverse voltage with
   an adequate margin to the maximum input voltage.
 	
   A diode with a low forward voltage and short reverse recovery
   time will provide high efficiency.
	When V_{IN} = 36 V and Io = (max.) 2 A,
	
	Select a diode of rated current of 2 A or more and rated
	withstand voltage of 36 V or more.

5. Selection of input capacitor
   Two capacitors, ceramic capacitor C_{IN} and bypass capacitor C,
   should be inserted between the V_{IN} and GND.Be sure to insert
   a ceramic capacitor of 1 to 10 μF for the C. The capacitor C
   should have a low ESR and a significantly large ripple current.
   The ripple current I_{RMS} can be obtained
   by the following formula:
 	
   $$I_{RMS}=I_O \times \sqrt{V_O \times (V_{in}-V_O)/ V_{in}^2}$$
 	
   Select capacitors that can accept this ripple current.
   If the capacitance of CIN and C is not optimum,
   the IC may malfunction.
	When V_{IN} = 13.2 V, Vo = 5 V, and Io = 1 A,
	
	$$I_{RMS}=1 \times \sqrt{5 \times (13.2-5)/(13.2)^2}$$
	   $=0.485$
	
	$\underline{I_{RMS}=0.485A}$

6. Setting of oscillation frequency
   Referring Fig. 34 and Fig. 35 on the following page, select R
   for the oscillation frequency to be used. Furthermore,
   in order to eliminate noises, be sure to connect ceramic
   capacitors of 0.1 to 1.0 μF in parallel.	

7. Setting of phase compensation (Rc and Cc)
   The phase margin can be set through inserting a capacitor or
   a capacitor and resistor between the INV pin and the FB pin.
   Each set value varies with the output coil, capacitance,
   I/O voltage, and load. Therefore, set the phase compensation
   to the optimum value according to these conditions.
    (For details, refer to Application circuit on page 11.)
   If this setting is not optimum, output oscillation may result.	

* The set values listed above are all reference values. On the actual mounting of the IC, the characteristics may vary with the routing of wirings
   and the types of parts in use. In this connection, it is recommended to thoroughly verify these values on the actual system prior to use.
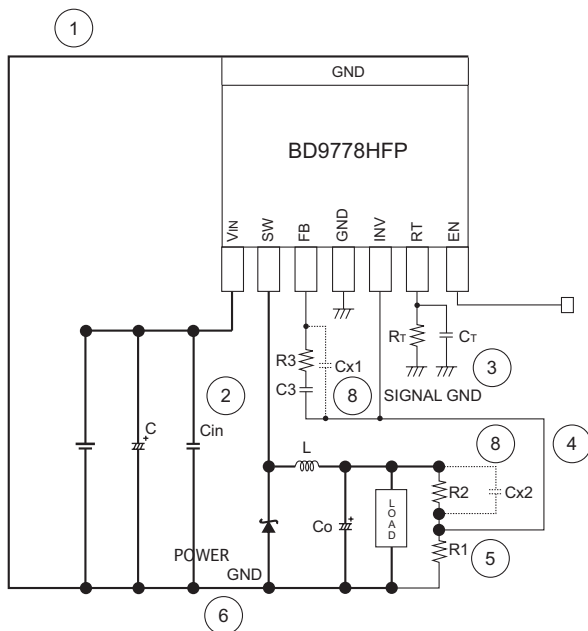
● Directions for pattern layout of PCB

① Arrange the wirings shown by heavy lines as short as possible
   in a broad pattern.
② Locate the input ceramic capacitor Cin as close to the VIN-GND pin
   as possible.
③ Locate the R_T and C_T as close to the GND pin as possible.
④ Locate the R1 and R2 as close to the INV pin as possible,
   and provide the shortest wiring from the R1 and R2 to the INV pin.
⑤ Locate the R1 and R2 as far away from the L as possible.
⑥ Separate POWER GND(Schottky diode, I/O capacitor's GND)
   and SIGNAL GND(R_T, C_T's GND), so that SW noise don't have an effect
   on SIGNAL GND at all.
⑦ Design the POWER wire line as wide and short as possible.
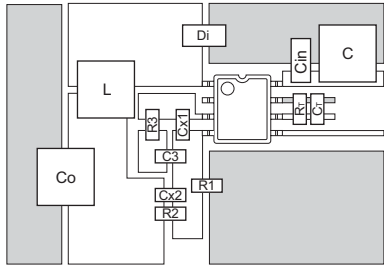⑧ Additional pattern for Cx1 and Cx2 expand compesation flexibility.
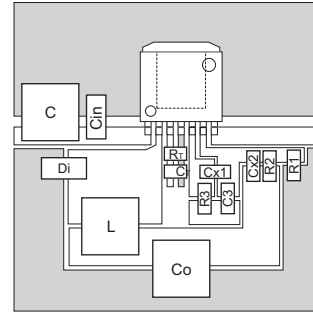
Fig.31

Fig.32 BD9001F reference layout pattern

Fig.33 BD9781HFP reference layout pattern

※ As shown above, design the GND pattern as large area as possible within inner layer.
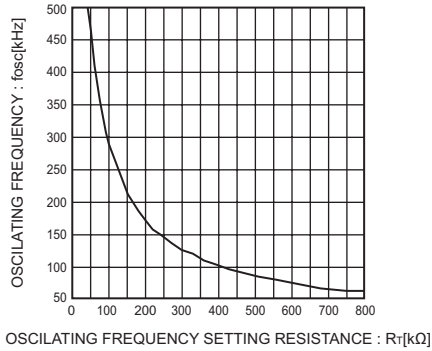※ Gray zones indicate GND.

Fig.34 RT vs fOSC (BD9781HFP/BD9778F/HFP)

※Oscillation frequency's graph value is Typical value, oscillation frequency is necessary to consider ±20% as dispersion.
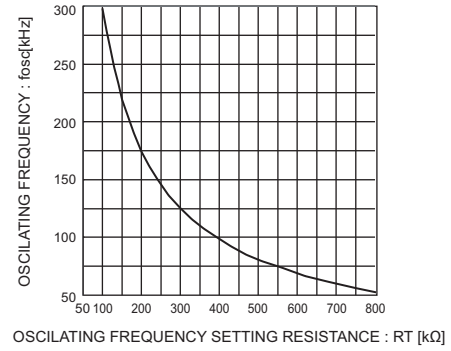

Fig.35 RT vs fOSC (BD9001F)

● Phase compensation setting procedure

1.   Application stability conditions

The following section describes the stability conditions of the negative feedback system.
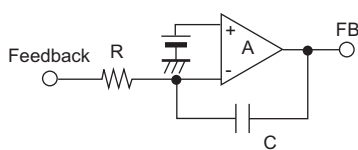
Since the DC/DC converter application is sampled according to the switching frequency, GBW (frequency at 0-dB gain) of the overall system should be set to 1/10 or less of the switching frequency. The following section summarizes the targeted characteristics of this application.

・   At a 1 (0-dB) gain, the phase delay is 150˚ or less (i.e., the phase margin is 30˚ or more).
・   The GBW for this occasion is 1/10 or less of the switching frequency.

Responsiveness is determined with restrictions on the GBW. To improve responsiveness, higher switching frequency should be provided.

Replace a secondary phase delay (-180˚) with a secondary phase lead by inserting two phase leads, to ensure the stability through the phase compensation. Furthermore, the GBW (i.e., frequency at 0-dB gain) is determined according to phase compensation capacitance provided for the error amplifier. Consequently, in order to reduce the GBW, increase the capacitance value.

(1) Typical integrator (Low pass filter)

(2) Open loop characteristics of integrator
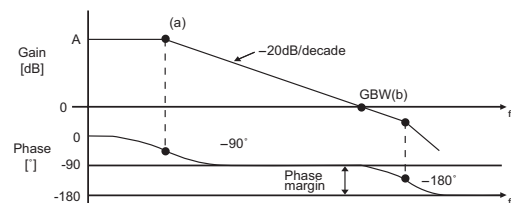

Point (a) $fa = \dfrac{1}{2\pi RCA}$ [Hz]

Point (b) $fb = GBW = \dfrac{1}{2\pi RC}$ [Hz]

Since the error amplifier is provided with (1) or (2) phase compensation, the low pass filter is applied. In the case of the DC/DC converter application, the R becomes a parallel resistance of the feedback resistance.

2. For output capacitors having high ESR, such as electrolyte capacitor

For output capacitors that have high ESR (i.e., several Ω), the phase compensation setting procedure becomes comparatively simple. Since the DC/DC converter application has a LC resonant circuit attached to the output, a -180° phase-delay occurs in that area. If ESR component is present, howeve r, a +90° phase-lead occurs to shift the phase delay to -90°. Since the phase delay should be set within 150°, it is a very effective method but tends to increase the ripple component of the output voltage.
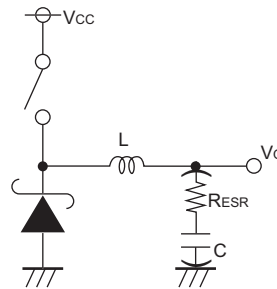
(1) LC resonant circuit
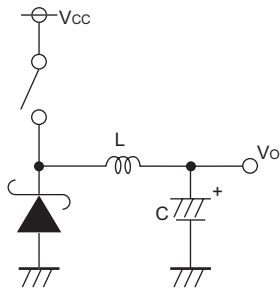
(2) With ESR provided

$$fr = \frac{1}{2\pi\sqrt{LC}} \text{ [Hz]}$$
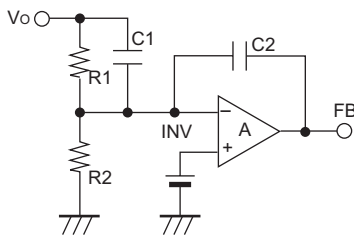
At this resonance point, a -180° phase-delay occurs.

$$fr = \frac{1}{2\pi\sqrt{LC}} \text{ [Hz]: Resonance point}$$

$$f_{ESR} = \frac{1}{2\pi\ R_{ESR}C} \text{ [Hz]: Phase lead}$$
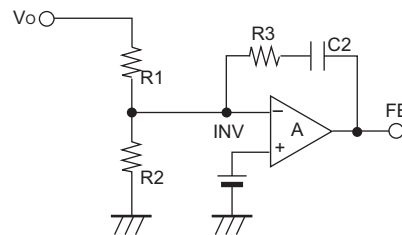
A -90° phase-delay occurs.

According to changes in phase characteristics, due to the ESR, only one phase lead should be inserted. For this phase lead, select either of the methods shows below:

(3) Insert feedback resistance in the C.

(4) Insert the R3 in integrator.

$$\text{Phase lead: } f_Z = \frac{1}{2\pi\ C1R1} \text{ [Hz]}$$

$$\text{Phase lead: } f_Z = \frac{1}{2\pi\ C2R3} \text{ [Hz]}$$

To cancel the LC resonance, the frequency to insert the phase lead should be set close to the LC resonant frequency. The settings above have are estimated. Consequently, the settings may be adjusted on the actual system. Furthermore, since these characteristics vary with the layout of PCB loading conditions, precise calculations should be made on the actual system.

3. For output capacitors having low ESR, such as low impedance electrolyte capacitor or OS-CON

In order to use capacitors with low ESR (i.e., several tens of mΩ), two phase-leads should be inserted so that a -180° phase-delay, due to LC resonance, will be compensated. The following section shows a typical phase compensation procedure.

(1) Phase compensation with secondary phase lead
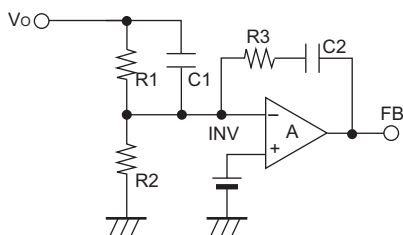
$$\text{Phase lead: } f_{Z1} = \frac{1}{2\pi\ R1C1} \text{ [Hz]}$$

$$\text{Phase lead: } f_{Z2} = \frac{1}{2\pi\ R3C2} \text{ [Hz]}$$

$$\text{LC resonant frequency: } fr = \frac{1}{2\pi\sqrt{LC}} \text{ [Hz]}$$

To set phase lead frequency, insert both of the phase leads close to the LC resonant frequency. According to empirical rule, setting the phase lead frequency f $_{Z2}$ with R3 and C2 lower than the LC resonant frequency fr, and the phase lead frequency f$_{Z1}$ with the R1 and C1 higher than the LC resonant frequency fr, will provide stable application conditions.

<Reference> Measurement of open loop of DC/DC converter

To measure the open loop of DC/DC converter, use the gain phase analyzer or FRA to measure the frequency characteristics.
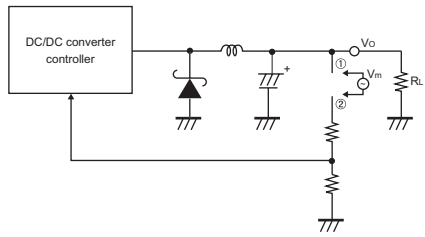

<Procedure>
1. Check to ensure output causes no oscillation at the maximum load in closed loop.
2. Isolate (1) and (2) and insert Vm (with amplitude of approximately 100 mVpp).
3. Measure (probe) the oscillation of (1) to that of (2).

Furthermore, the phase margin can also be measured with the load responsiveness.
Measure variations in the output voltage when instantaneously changing the load from no load to the maximum load.
Even though ringing phenomenon is caused, due to low phase margin, no ringing takes place. Phase margin is provided. However, no specific phase margin can be probed.
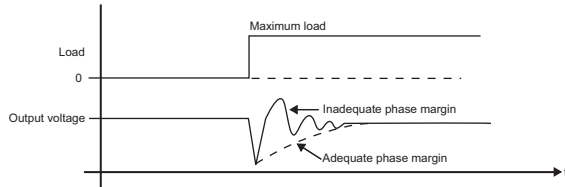
● Heat loss

For thermal design, be sure to operate the IC within the following conditions.
(Since the temperatures described hereunder are all guaranteed temperatures, take margin into account.)
1. The ambient temperature Ta is to be 125ºC or less.
2. The chip junction temperature Tj is to be 150ºC or less.

The chip junction temperature Tj can be considered in the following two patterns:

To obtain Tj from the IC surface temperature Tc in the actual use state,
$$Tj = Tc + \theta_{j-c} \times W$$

<Reference value> θ_{j-c} : HRP7   7 ℃/W
                         SOP8 32.5 ℃/W

To obtain Tj from the ambient temperature Ta
$$Tj = Ta + \theta_{j-a} \times W$$

<Reference value> θ_{j-a} : HRP7 89.3 ℃/W   Single piece of IC
                         54.3 ℃/W   2-layer PCB (Copper foil area on the front side of PCB: 15×15 mm^2)
                         22.7 ℃/W   2-layer PCB (Copper foil area on the front side of PCB: 70×70 mm^2)
                         PCB size: $70 \times 70 \times 1.6$ mm^3 (PCB incorporates thermal via.)
                         Copper foil area on the front side of PCB: 10.5×10.5 mm^2
                   SOP8 222.2 ℃/W   Single piece of IC
                         181.8 ℃/W   1-layer PCB
                         PCB size: $70 \times 70 \times 1.6$ mm^3

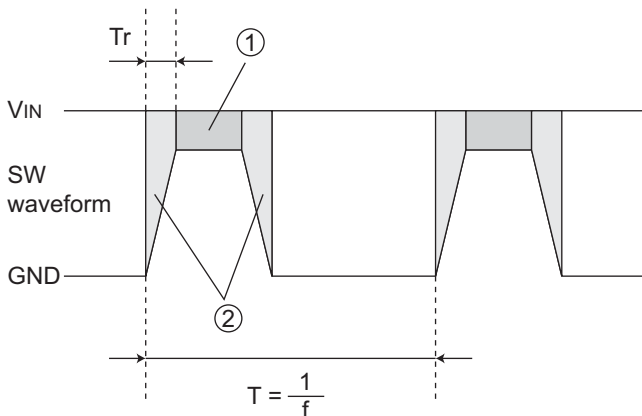The heat loss W of the IC can be obtained by the formula shown below:

$$W = Ron \times Io^2 \times \frac{Vo}{V_{IN}} + V_{IN} \times Icc + Tr \times V_{IN} \times Io \times f$$

Ron: ON resistance of IC (refer to pages 4 and 5.) Io: Load current Vo: Output voltage
V$_{IN}$: Input voltage Icc: Circuit current (Refer to pages 2 and 3)
Tr: Switching rise/fall time (Approximately 40 nsec)
f : Oscillation frequency

① Ron $\times$ Io^2

② $2 \times \frac{1}{2} \times Tr \times \frac{1}{T} \times V_{IN} \times Io$

   $= Tr \times V_{IN} \times Io \times f$
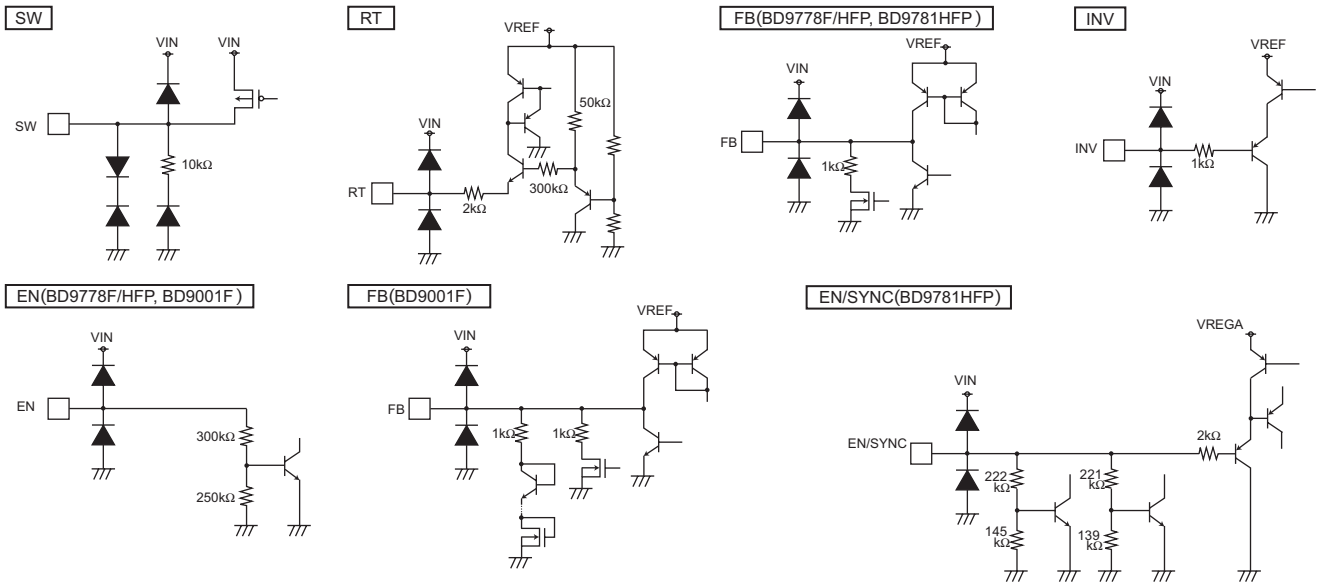
$$T = \frac{1}{f}$$

Fig.36 Equivalent circuit

● Notes for use

1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses. Furthermore, don't turn on the IC with a fast rising edge of V_{IN}. (rise time << 10V / µsec)

2) GND potential

GND potential should maintain at the minimum ground voltage level. Furthermore, no terminals should be lower than the GND potential voltage including an electric transients.

3) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if positive and ground power supply terminals are reversed. The IC may also be damaged if pins are shorted together or are shorted to other circuits power lines.

5) Operation in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6) Inspection with set printed circuit board

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to, or removing it from a jig or fixture, during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting and storing the IC.
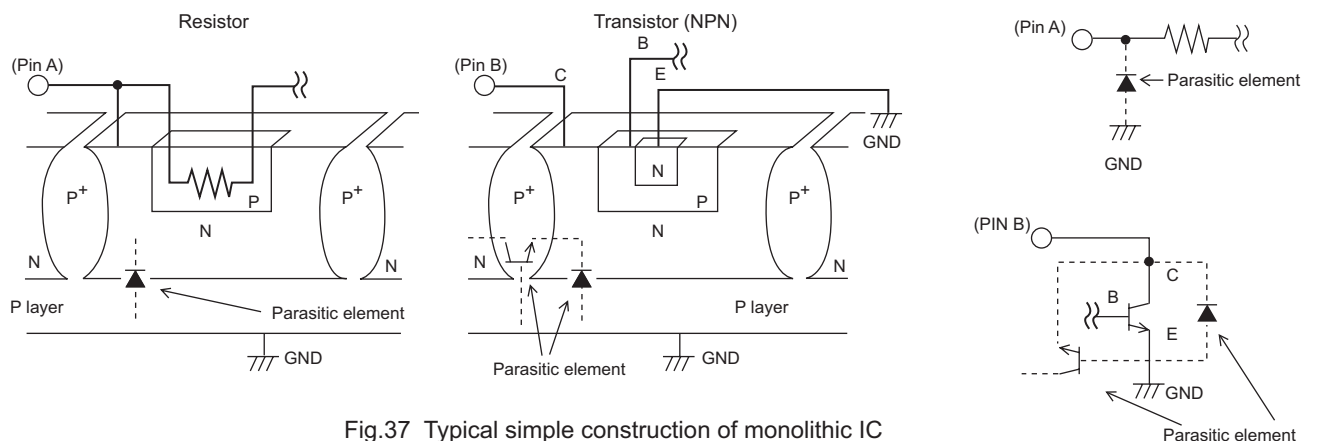

Fig.37 Typical simple construction of monolithic IC

7) IC pin input (Fig. 37)

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements to keep them isolated.
P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:
  When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
  When Pin B > GND > Pin A, the P-N junction operates as a parasitic transistor. Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage toan input pin, should not be used.

8) Ground wiring pattern

It is recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB, so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Prevent fluctuations in the GND wiring pattern of external parts.

9) Temperature protection (thermal shut down) circuit

This IC has a built-in temperature protection circuit to prevent the thermal destruction of the IC. As described above, be sure to use this IC within the power dissipation range. Should a condition exceeding the power dissipation range continue, the chip temperature Tj will rise to activate the temperature protection circuit, thus turning OFF the output power element. Then, when the tip temperature Tj falls, the circuit will be automatically reset. Furthermore, if the temperature protection circuit is activated under the condition exceeding the absolute maximum ratings, do not attempt to use the temperature protection circuit for set design.

10) On the application shown below, if there is a mode in which V_{IN} and each pin potential are inverted, for example, if the V_{IN} is short-circuited to the Ground with external diode charged, internal circuits may be damaged. To avoid damage, it is recommended to insert a backflow prevention diode in the series with V_{IN} or a bypass diode between each pin and V_{IN}.
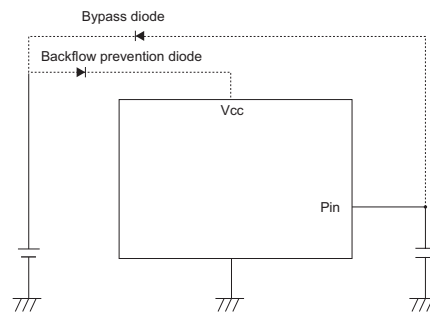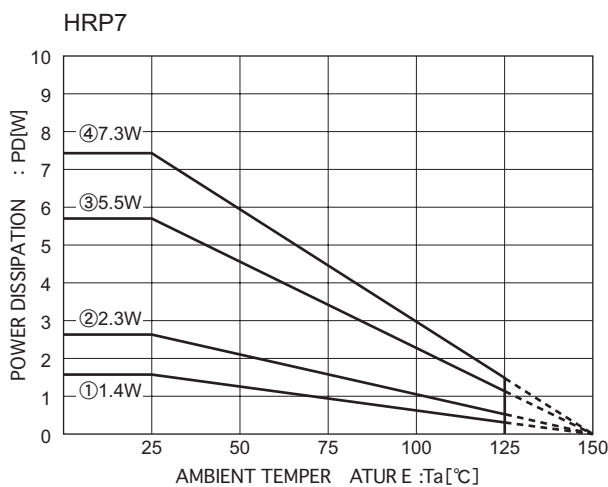
Fig.35

● Thermal derating characteristics

HRP7

SOP8

① Single piece of IC
  PCB size: 70 x 70 x 1.6 mm^3 (PCB incorporates thermal via.)
  Copper foil area on the front side of PCB: 10.5 x 10.5 mm2
② 2-layer PCB (Copper foil area on the reverse side of PCB: 15 x 15 mm^2)
③ 2-layer PCB (Copper foil area on the reverse side of PCB: 70 x 70 mm^2)
④ 4-layer PCB (Copper foil area on the reverse side of PCB: 70 x 70 mm^2)
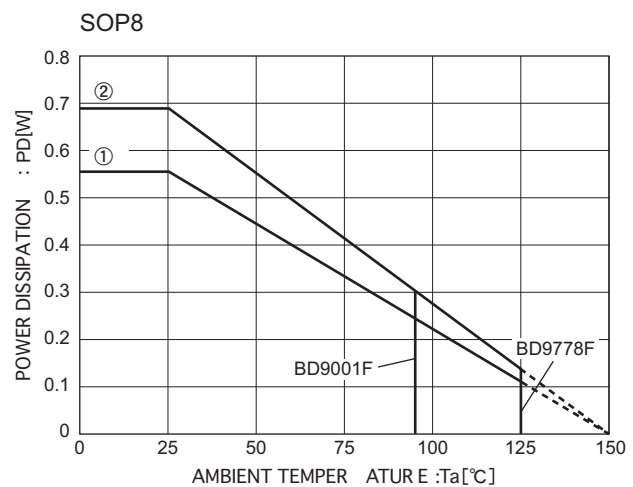
① Single piece of IC
② When mounted on ROHM standard PCB
  (Glass epoxy PCB of 70 mm x 70 mm x 1.6 mm)

Fig.39   Fig.40

● Selection of order type

| B | D | | 9 | 7 | 7 | 8 | | H | F | P | - | T | R |

Part No.

Part No.
9778 = 36V/2A
9781 = 36V/4A
9001 = 50V/2A
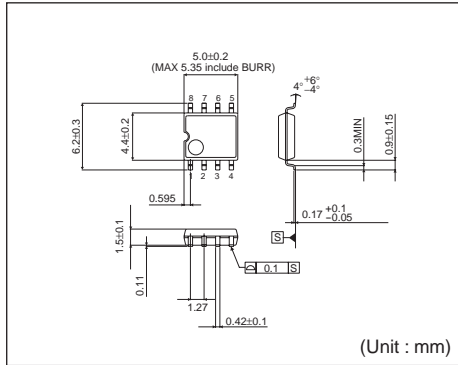
Package
F = SOP8
HFP = HRP7
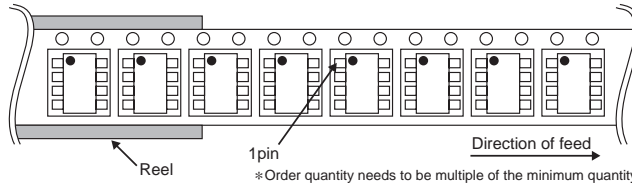
Taping type
E2 = Reel-type embossed carrier tape (SOP8)
TR = Reel-type embossed carrier tape (HRP7)

SOP8

(Unit : mm)
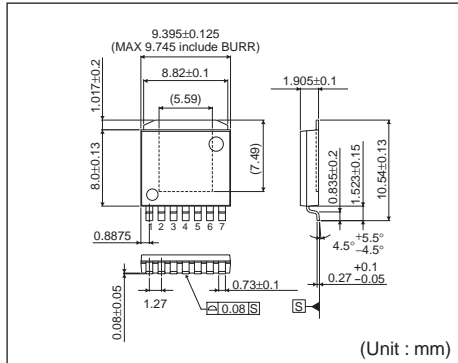
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

1pin

Reel

Direction of feed

＊Order quantity needs to be multiple of the minimum quantity.

HRP7

(Unit : mm)

<Tape and Reel information>

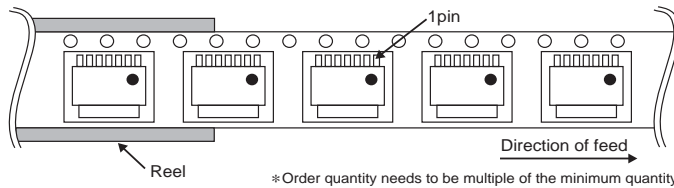| Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)

1pin

Reel

Direction of feed

＊Order quantity needs to be multiple of the minimum quantity.

ご注意

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CLASSⅢ	CLASSⅢ	CLASSⅡb	Ⅲ類
CLASSⅣ		CLASSⅢ	

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   - ②冗長回路等を設けて単一故障では危険が生じないようにシステムとしての安全を確保する。

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   - ②直射日光・屋外暴露、塵埃中でのご使用
   - ③潮風、Cl_2、H_2S、NH_3、SO_2、NO_2 等の腐食性ガスの多い場所でのご使用
   - ④静電気や電磁波の強い環境でのご使用
   - ⑤発熱部に近接した取付け及び当製品に近接してビニール配線等、可燃物を配置する場合。
   - ⑥本製品を樹脂等で封止、コーティングしてのご使用。
   - ⑦はんだ付けの後に洗浄を行わない場合(無洗浄タイプのフラックスを使用された場合も、残渣の洗浄は確実に行うことをお薦め致します)、又ははんだ付け後のフラックス洗浄に水又は水溶性洗浄剤をご使用の場合。
   - ⑧本製品が結露するような場所でのご使用。

4. 本製品は耐放射線設計はなされておりません。

5. 本製品単体品の評価では予測できない症状・事態を確認するためにも、本製品のご使用にあたってはお客様製品に実装された状態での評価及び確認をお願い致します。

6. パルス等の過渡的な負荷（短時間での大きな負荷）が加わる場合は、お客様製品に本製品を実装した状態で必ずその評価及び確認の実施をお願い致します。また、定常時での負荷条件において定格電力以上の負荷を印加されますと、本製品の性能又は信頼性が損なわれるおそれがあるため必ず定格電力以下でご使用ください。

7. 許容損失(Pd)は周囲温度(Ta)に合わせてディレーティングしてください。また、密閉された環境下でご使用の場合は、必ず温度測定を行い、ディレーティングカーブ範囲内であることをご確認ください。

8. 使用温度は納入仕様書に記載の温度範囲内であることをご確認ください。

9. 本資料の記載内容を逸脱して本製品をご使用されたことによって生じた不具合、故障及び事故に関し、ロームは一切その責任を負いません。

実装及び基板設計上の注意事項

1. ハロゲン系（塩素系、臭素系等）の活性度の高いフラックスを使用する場合、フラックスの残渣により本製品の性能又は信頼性への影響が考えられますので、事前にお客様にてご確認ください。

2. はんだ付けはリフローはんだを原則とさせて頂きます。なお、フロー方法でのご使用につきましては別途ロームまでお問い合わせください。
   詳細な実装及び基板設計上の注意事項につきましては別途、ロームの実装仕様書をご確認ください。

応用回路、外付け回路等に関する注意事項

1. 本製品の外付け回路定数を変更してご使用になる際は静特性のみならず、過渡特性も含め外付け部品及び本製品のバラツキ等を考慮して十分なマージンをみて決定してください。

2. 本資料に記載された応用回路例やその定数などの情報は、本製品の標準的な動作や使い方を説明するためのもので、実際に使用する機器での動作を保証するものではありません。従いまして、お客様の機器の設計において、回路やその定数及びこれらに関連する情報を使用する場合には、外部諸条件を考慮し、お客様の判断と責任において行ってください。これらの使用に起因しお客様又は第三者に生じた損害に関し、ロームは一切その責任を負いません。

静電気に対する注意事項

本製品は静電気に対して敏感な製品であり、静電放電等により破壊することがあります。取り扱い時や工程での実装時、保管時において静電気対策を実施の上、絶対最大定格以上の過電圧等が印加されないようにご使用ください。特に乾燥環境下では静電気が発生しやすくなるため、十分な静電対策を実施ください。（人体及び設備のアース、帯電物からの隔離、イオナイザの設置、摩擦防止、温湿度管理、はんだごてのこて先のアース等）

保管・運搬上の注意事項

1. 本製品を下記の環境又は条件で保管されますと性能劣化やはんだ付け性等の性能に影響を与えるおそれがありますのでこのような環境及び条件での保管は避けてください。
   ①潮風、Cl_2、H_2S、NH_3、SO_2、NO_2等の腐食性ガスの多い場所での保管
   ②推奨温度、湿度以外での保管
   ③直射日光や結露する場所での保管
   ④強い静電気が発生している場所での保管

2. ロームの推奨保管条件下におきましても、推奨保管期限を経過した製品は、はんだ付け性に影響を与える可能性があります。推奨保管期限を経過した製品は、はんだ付け性を確認した上でご使用頂くことを推奨します。

3. 本製品の運搬、保管の際は梱包箱を正しい向き（梱包箱に表示されている天面方向）で取り扱いください。天面方向が遵守されずに梱包箱を落下させた場合、製品端子に過度なストレスが印加され、端子曲がり等の不具合が発生する危険があります。

4. 防湿梱包を開封した後は、規定時間内にご使用ください。規定時間を経過した場合はベーク処置を行った上でご使用ください。

製品ラベルに関する注意事項

本製品に貼付されている製品ラベルに QR コードが印字されていますが、QR コードはロームの社内管理のみを目的としたものです。

製品廃棄上の注意事項

本製品を廃棄する際は、専門の産業廃棄物処理業者にて、適切な処置をしてください。

外国為替及び外国貿易法に関する注意事項

本製品は外国為替及び外国貿易法に定める規制貨物等に該当するおそれがありますので輸出する場合には、ロームにお問い合わせください。

知的財産権に関する注意事項

1. 本資料に記載された本製品に関する応用回路例、情報及び諸データは、あくまでも一例を示すものであり、これらに関する第三者の知的財産権及びその他の権利について権利侵害がないことを保証するものではありません。従いまして、上記第三者の知的財産権侵害の責任、及び本製品の使用により発生するその他の責任に関し、ロームは一切その責任を負いません。

2. ロームは、本製品又は本資料に記載された情報について、ローム若しくは第三者が所有又は管理している知的財産権その他の権利の実施又は利用を、明示的にも黙示的にも、お客様に許諾するものではありません。

その他の注意事項

1. 本資料の全部又は一部をロームの文書による事前の承諾を得ることなく転載又は複製することを固くお断り致します。

2. 本製品をロームの文書による事前の承諾を得ることなく、分解、改造、改変、複製等しないでください。

3. 本製品又は本資料に記載された技術情報を、大量破壊兵器の開発等の目的、軍事利用、あるいはその他軍事用途目的で使用しないでください。

4. 本資料に記載されている社名及び製品名等の固有名詞は、ローム、ローム関係会社若しくは第三者の商標又は登録商標です。

一般的な注意事項

1. 本製品をご使用になる前に、本資料をよく読み、その内容を十分に理解されるようお願い致します。本資料に記載される注意事項に反して本製品をご使用されたことによって生じた不具合、故障及び事故に関し、ロームは一切その責任を負いませんのでご注意願います。

2. 本資料に記載の内容は、本資料発行時点のものであり、予告なく変更することがあります。本製品のご購入及びご使用に際しては、事前にローム営業窓口で最新の情報をご確認ください。

3. ロームは本資料に記載されている情報は誤りがないことを保証するものではありません。万が一、本資料に記載された情報の誤りによりお客様又は第三者に損害が生じた場合においても、ロームは一切その責任を負いません。